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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,596	02/04/2004	Alfredo Herrera	16550ROUS01U	3440

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JOHN C. GORECKI, ESQ.
P.O BOX 553
CARLISLE, MA 01741

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,596	HERRERA, ALFREDO	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 12-15* is/are rejected.

7)☒ Claim(s) *6-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/771,596 and Preliminary Amendment filed on 8/23/2004. Claims 1-15 remain pending in the application. Note: applicant is requested submitted all references cited. Since no references, Examiner has not considered these references at this time.

Drawings

2. The drawings are objected to because Figure 3B filed on Aug. 23, 2004 lacks labeling "Replacement Sheet" on top left of the sheet. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. The subject matter of this application admits of illustration by a drawing to facilitate understanding of the invention. Applicant is required to furnish a drawing under 37 CFR 1.81(c). No new matter may be introduced in the required drawing. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-4 and 12-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention appears to be to an abstract idea because the claimed invention does not result in a physical transformation nor does it appears to provide a useful, concrete and tangible result.

Therefore, claims 1-4 and 12-15 appear non-statutory because they are just an abstract idea. There is no concrete and tangible result. For example, the steps of calculating or translation are just an abstract idea.

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-4 and 12-15 are rejected under 35 U.S.C. 101 because the claimed invention is not supported by either a credible asserted utility or a well established utility.

The claimed invention appears to be to an abstract idea because the claimed invention does not result in a physical transformation nor does it appears to provide a useful, concrete and tangible result. Therefore, claims 1-4 and 12-15 appear non-statutory.

Claims 1-4 and 12-15 are also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a credible asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1 and 14-15 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the steps to show

the calculating without substantially intervention from a human operator (claim 1) and translation of a file into a format usable to program a programmable logic device and iterate translation to achieve an optimized format.

Other dependent claims which are not specifically cited above are also rejected because of the deficiencies of their respective parent claims.

Claim Objections

7. Claims 1, 2 and 3 are objected to because of the following informalities: claim 1, line 1, "the design" should be changed to --a design--; claim 2, line 2, one of "hollowed" should be deleted (duplicate); claim 3, phrase "capable of" is not an a defined claim language. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-5 and 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahanessians et al. (6,401,230 B1).

10. As to claim 1, Ahanessians et al. teach a method for generating customized megafunctions. The method comprising a software module referred to as "plug-ins" associates with megafunctions written in any Hardware Description Language (HDL, RTL, VHDL, Verilog) to provide rich parameterization. To the user, the plug-ins

presents a "wizard" interface allowing selection or setting or any number of important parameters for a particular megafunction. To the design compiler, parameterized megafunctions instantiated via a plug-in appears non-parameterized functions of a type that may be easily handled by VHDL and Verilog compilers. Pug-ins plug into a compiler or an application associated with the compiler, sometimes referred to as a plug-in manager. The plug-in manager /creates compilable files (compilable variation of parameterized function blocks for electronic designs) from user-defined parameter settings passed by the plug-ins (see summary). This compilable variation, when used with associated parameterized function blocks (design implementation files), allow the compiler to create unambiguous circuit blocks forming parts of electronic designs. Each plug-in associated with different functional blocks (design implementation files) and a plug-in manager handle information from many different plug-ins to create compilable variation of parameterized function blocks for electronic designs (a set of design output files) (see summary). The plug-in manager may make connections to provide a single design suitable for the configurations and connections specified by the user. Note that unlike a traditional design process, this design process does not require that the user/developer make the connections between the magafunctions manually (col. 8, lines 1-6). The plug-in may ultimately generate the appropriate connections between the filter elements (without specific user input) and may simplify the functioning of the individual elements depending upon the specified parameters (col. 7 lines 42-63). Fig. 11 shows a generated programmable logic device (PLD) (col. 16, lines 43-67). In addition, Fig. 10 the EDA tool including logic synthesizer, technology mapper,

placement and routing performing the calculating step without substantially intervention from a human operator.

11. As to claim 2, Ahanessians et al. teach the design implementation files comprise a hollowed netlist (netlist of each megafunction for example 303, 305, 307 in Fig. 3A), a filled netlist (netlist of custom wrapper Fig. 3A or Fig. 3B), data-path constraints (data-path constraints between megafunctions), and design constraints (complete design constraint of each megafunction or whole design constraints) (col. 6 lines 51-67; col. 7 lines 1-7; col. 9 lines 17-38).

12. As to claim 3, Ahanessians et al. teach this compilable variation, when used with associated parameterized function blocks (design implementation files), allow the compiler to create unambiguous circuit blocks forming parts of electronic designs. The compiler provides output files that are mapping to a target hardware design, thus the output files are used to program the programmable logic devices.

13. As to claim 4, Ahanessians et al. teach an EDA including design compiler associated with wizard manager and plug-ins to generate a set of scripts, setup files, and tool lineup files for use in programming the programmable logic devices or generate a custom design (Fig. 2, 4 and 10; col. 6 lines 51-67; col. 7 lines 1-7; col. 7 lines 64-67; col. 8 lines 1-17; col. 9 lines 7-38; col. 11 lines 4-67).

14. As to claim 5, Ahanessians et al. the limitations of the claim are common practice in physical layout design performed by EDA tools (Fig. 10) including synthesis and placement and routing (col. 16 lines 20-67).

15. As to claim 12, Ahanessians et al. teach programmable logic devices (col. 16 lines 43-67). Note that the programmable logic device is a Field Programmable Gate Array.

16. As to claim 13, Ahanessians et al. teach parameterized function block is provided in a hardware description language (HDL, VHDL, AHDL, Verilog) (col. 6 lines 51-60). Note the HDL files are subject to Register Transfer Language (RTL) Synthesis.

17. As to claim 14, Ahanessians et al. teach a computer comprising design software (Fig. 2, design compiler, plug-ins, wizard manager) to translate a file created using at least one of a hardware descriptor language and a register transfer language into a format usable to program a programmable logic device (at least see summary).

18. As to claim 15, Ahanessians et al. teach the EDA tools configured to iterate the translation to achieve an optimized format (col. 9 lines 17-37).

19. Claims 1-5 and 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Jain et al. (6,484,292 B1).

20. As to claim 1, Jain et al. teach a method for automating a design of programmable logic devices comprising obtaining design implementation files (Fig. 2, design implementation files); and calculating a set of design output files from the design implementation files without substantial intervention from a human operator (the process is controlled by software elements front-end synthesis, build and fitter). In addition, the placement and routing software is also involved in performing the calculating step.

21. As to claim 2, the design implementation files (Fig. 2) comprising a hollowed netlist (a netlist associated with CO design implementation), a filled netlist (a netlist associated with Cn design implementation), data-path constraints (convert any optimized global signals of CO mapped to the global I/O pins, Fig. 4) and design constraints (constraints, Fig. 2).

22. As to claim 3, Jain et al. teach the output files (POs of Sn are used to re-synthesize attribute) and output of design implementation is used for placement and routing for PLDs (Fig. 4).

23. As to claim 4, in order to perform placement and routing of PLDs a set of scripts, setup files, tool lineup files are needed (Fig. 4).

24. As to claim 5, Jain et al. teach that changes are made to these control options, only the logic with re-synthesize attribute or the logic that does not meet timing specifications is affected by the control options and re-optimized and re-mapped, while logic of unaffected elements is neither re-optimized nor re-mapped (col. 5 line 62 to col. 6 line 56). Note that initially placement of logic groups, estimating resource usage, estimating timing and filling logic groups with primitive information are common practice during placement and routing performing by placement and routing as taught by Jain (Fig. 4).

25. As to claim 12-13, Jain et al. teach a hardware design description (HDL) (col. 2 lines 50-63). Note that the HDL is known to be subject to RTL synthesis. Jain et al. teach implementing circuit designs including PLDs (col. 3 lines 1-7). Note that a FPGA is a common device of PLDs.

26. As to claims 14-15, Jain et al. teach a software module (Fig. 2 and 4) for use to program a program a programmable logic device by sequentially modifications (translations) to achieve an optimized format (col. 3 lines 25-55; col. 5 line 62 to col. 6 line 55).

Allowable Subject Matter

27. Claims 6-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and rewritten to overcome rejections under 101, 112/1 and 2 as described above. For example, the prior art of record does not teach or fairly suggest initially placing logic groups comprising merging the hollowed netlist with the design constraints and iterating until the placement of the logic groups meets the design constraints as recited in claim 6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER